Design and Demonstration of a Passive, Broadband Equalizer for an SLED

Chris Brinton, Matthew Wharton, and Allen Katz

Introduction

Wavelength Division Multiplexing Passive Optical Networks (WDM PONs) have recently been commercialized by vendors including LG, Nortel and Alcatel-Lucent, and are considered by many to be higher performance than Time Division Multiplexing (TDM) PON systems, which are widely deployed today. Adding broadcast service to TDM PON is relatively simple, as it requires the addition of a single downstream wavelength. For WDM PON it is more complex, since the 1:N Arrayed Waveguide Grating (AWG) used at the remote node requires a broadband light source to broadcast to N users. AT&T Labs Research and Development in Middletown, NJ, has investigated the possibility of overlaying video and Gigabit Ethernet (GbE) through the direct modulation of a super luminescent light emitting diode (SLED), that acts as a broadband source (similar to an LED) with high power (similar to a laser source), which when coupled with an optical bandpass filter to eliminate wavelength interference with other channels, can excite the wavelengths of a 1:32 AWG. A high level block diagram of their proposed system, from central office to user, is shown in Figure 1.

One shortcoming of this technique is that the SLED has a poor modulation response. To this end, we have designed and taken measurements on a small scale, passive gain equalizer implemented on a printed circuit board (PCB), which we shall refer to in this paper as a compensator. Throughout this paper, we rely solely on AWR's Microwave Office for simulations.

Compensator Design

In order to design the compensator, we consider the electrical characteristics of the SLED. By modeling it as a two-port network as shown in Figure 2, we can measure the S-

parameters to obtain its gain response. With $\mathbf{a}_1$ and $\mathbf{a}_2$ representing the incident waves and $\mathbf{b}_1$ and $\mathbf{b}_2$ representing the reflected waves on ports 1 and 2, respectively, we have from S-parameter theory that

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{1}$$

and thus

$$\frac{b_2}{a_1}|_{a_2=0} = S_{21}, \tag{2}$$

which is a measure of the 2-port network gain in a system that has input and output impedances matched to the characteristic impedance $Z_0 = 50\ \Omega$.

The two-port S-parameters of SLED were measured using a vector network analyzer (VNA), and a bias tee at 5 V and 142 mA was used to obtain the recommended operating conditions. The magnitude and phase response measurements of the SLED are shown in Figure 3. The phase response has a linear regression correlation coefficient of roughly unity, corresponding to the almost constant group delay $\tau_g(f) \approx 35\,ns$ of the SLED. With the responses shown, it was concluded that only the magnitude response of the SLED required alteration. Therefore, a passive compensator should, through attenuation at lower frequencies, emulate the following response:

$$G_{comp}(f) = \begin{cases} \frac{A}{|G|_{SLED}(f)} e^{-j2\pi f t_0}, & \sim DC < f < 650\ MHz \\ \frac{A}{\left(\frac{f}{650x10^6}\right) * |G|_{SLED}(f)} e^{-j2\pi f t_0}, & 650\ MHz < f < 1.25\ GHz \end{cases} \tag{3}$$

In equation (3), A is a variable gain constant. The condition that the resultant response of the filter roll off exactly as a single pole low pass filter after 650 MHz is an approximate specification – the results were deemed to be satisfactory as long as the overall response begins to consistently decrease in magnitude after reaching approximately 650 MHz at a rate of no

greater than 50 dB/decade.

Given the necessity of obtaining sharp responses within the 650 MHz to 850 MHz range, highpass characteristics were required. Simultaneously, in order to pass components at DC without the use of active circuitry, another parallel section was needed that was capable of providing the necessary low frequency attenuation, without completely blocking the signal within these ranges. Finally, frequency selective band-attenuation sections were needed at the onset of the circuit to gain additional control over the sharpness of the highpass response. Excluding the effects of loading between each stage, a block diagram of the network is shown in Figure 4.

Development of the necessary components in the circuit was accomplished using a seventh-order LC high pass filter in parallel with a divider between a resistance and a resistance in series with an inductance. At the onset of the network, three RLC attenuation sections and a tee attenuator were placed for additional shaping of the highpass response. The resulting circuit, with ideal component values, is shown in Figure 5. The simulated response as compared to the ideal compensator response can be seen in Figure 11 (top). There is less than 1 dB of difference between the ideal gain response and the response shown up to ~ 940 MHz. The response begins to deviate by greater than 1 dB after 960 MHz, with a maximum deviation of ~2.8 dB at 1.25 GHz.

Before fabricating the compensator, it was necessary to develop a sophisticated model of the circuit to determine possible variation in the output response. First, commercially available SMT inductors were chosen from Digi-Key Corporation, since generally SMT inductors have less options, and are more prone to self-resonance (f_{res}) and equivalent series resistance (ESR) than SMT capacitors. The corresponding models used to simulate the effects of f_{res} and ESR are

shown in Figure 6. The calculations of C_d and R_s for the inductors employed the following equations:

$$C_d = \frac{1}{(2\pi f_{res})^2 L_{nom}} \quad (4)$$

$$R_s = \frac{X_L(f)}{Q(f)} \quad (5)$$

using the data provided in Table 1 for the chosen inductors. Similarly, (4) can be rearranged to calculate L_s from C_{nom}.

From the quality factor (Q) data given graphically as function of frequency (not shown), it was determined that for each of the inductors chosen, the value of R_s would have insignificant effects on the compensator response above 100 MHz, since the reactance was at least eight times as large. Near DC, the value of R_s became so small that it provided an approximate short circuit relative to the generally large resistances surrounding the inductors. Even so, the inductor model in Figure 6 was implemented in Microwave Office using a frequency-dependent resistance for R_s based upon the values of Q supplied by the manufacturer. The resultant circuit was simulated and plotted against the model with ideal component values (not shown). While the ESR and self-resonant characteristics were not seen to affect the designed response by more than a few dB, the inductor tolerances were seen to affect the compensator response by as much as 7 dB, as shown in Figure 7. Therefore, it was determined that measuring their actual values on a VNA was necessary in order to emulate the ideal response.

Once the inductors were received, they were soldered onto female flange SMA connectors, and their $\mathbf{S}_{11}$ characteristics were measured and displayed on a VNA's Smith Chart. The resistive and reactive components of the inductors were measured as a function of frequency from 300 kHz to 1.25 GHz. The reactance plot is shown in Figure 8, and linear regression was run on the reactive data for each inductor, all of which gave a correlation coefficient of $R^2 \geq$

0.99, with the exception of the 15 nH which had R^2 = 0.98. From the plots, the equivalent inductances can be calculated from

$$L = \frac{1}{2\pi} * \left(\frac{X(f)}{f\ (MHz)}\right) * 10^{-6}\ H. \quad (6)$$

The values calculated from equation (6) are shown in Table 2. It is important to note that despite the linearity of the reactance, each inductor is significantly larger than its nominal value.

The measured inductance values were imported into Microwave Office using the element ZFREQ, which allows for arbitrary definitions of resistance and reactance at specified frequencies, and uses a linear interpolation model at all points between. At this point, it was necessary to retune much of the circuit, due to the non-idealities and deviation in nominal values of the inductors. To accomplish this, the compensator was cascaded with the SLED's two-port model in Microwave Office, and the real-time tuning feature was used to tweak the components of the circuit while monitoring the resulting $|\mathbf{S}_{21}|$ response. For instance, it was necessary to place an 8.2 nH nominal (measured 9.34 nH) in parallel with each of the 1.5 and 1.8 nH inductors in order to bring them closer to the specified values. C5 and L6 were noticed to have had little effect on the frequency response and were eliminated from the circuit. The updated compensator schematic is shown in Figure 9. The expectation is that the compensator will yield a pass-band ripple of less than 1 dB, as shown in the simulation plot of Figure 14 (bottom).

Compensator Fabrication and Testing

After completing the simulations, the compensator was fabricated and tested. Eagle was used to generate the necessary Gerber files for the etching of the board. The substrate chosen was industry standard 62 mil-thick FR-4, which has little variation in its dielectric constant ε_r of 4.7 over the frequency range of interest, and a loss tangent $\delta = 0.017$. The copper signal traces used were 1 oz (1.4 mil), 35 mil wide with 7 mil isolation between the conductor and ground;

guaranteeing approximately 50 Ω (50.6 exact) traces. 12 mil diameter, round vias were placed around the components of the board (farther than 7 mil away). The input and output ports were reached through ~50Ω traces extended to the edge of the board for side-mount SMA connectors. For convenience of shape, and to leave enough room for additional SMT components if needed, a 2" x 2" board was chosen. The geometry used was coplanar waveguide (CPW) with ground. The routed Eagle board file and the fabricated compensator (built at Linearizer Technology in Hamilton, NJ) are shown in the top and bottom of Figure 10, respectively.

The measured compensator response, as compared to the designed and ideal responses, is shown in Figure 11. In the critical frequency range, from 0 to 650 MHz, the difference between of the maximum and minimum deviations between the ideal and measured responses gives the passband ripple. This value was determined to be approximately 6.7 dB, taking the difference between the deviation at 250 MHz and at 650 MHz, which was ~4 dB higher than desired. In addition, although the flatness of the high frequency response is not as critical, the measurements were between 5 and 6 dB lower than the expected response of the compensator from 590 to 885 MHz. This will cause the overall system to have this amount of additional roll-off when operating within this frequency range.

Compensator Error Analysis and Tuning

As a result of the poor correlation between the designed and measured responses (which, even as is, would significantly improve the high frequency response of the SLED), the next step was taken to determine possible causes for the deviations. Feasible explanations are that incorrect component values were shipped, or that incorrect components were drawn from the packages when soldering. The sharp decrease in response from ~400 to 600 MHz is controlled by the value of C6 in Figure 9. Changing this value to 5.1 pF makes the measured and simulated

responses agree over this band. At the highest frequencies, the value of C2 in the R2-L2-C2 band-attenuation section controls the sharpness of the response. Reducing this value to 5.1 pF makes the frequency responses from 1 to 1.25 GHz almost identical. In addition, the response drop that is expected to occur from 900 to 1010 MHz, a result of the R2-C2-L2 band-attenuation section, was not present in the measurements. This can be eliminated from the design by changing the value of R2 to 84.5 Ω (which is the nominal value of R1).

Another explanation for the lack of agreement between the responses is the tolerances on the component values. Most likely, at least some error was caused by deviation of the inductors from their nominal values, since the specific ones measured were seen to deviate largely, as shown in Table 2.

To correct the measured response, the compensator was tuned. Increasing C1 by adding a 2.7 pF capacitor in parallel had the desirable effect of bringing the frequency dip present from 950 – 1000 MHz in Figure 11 (top) to a lower frequency range while simultaneously increase its sharpness. R8 provided control over the low frequency attenuation, and therefore the ripple shown in this range was reduced by increasing its value to 39 Ω. The sharpness of the highpass response was improved by placing a 1 pF capacitor in parallel with C5. Finally, the reduction in the sharpness of the dip, now located at ~955 MHz, was accomplished by completely removing R3 from the circuit. The resulting response, as compared with the untweaked, designed, and ideal responses, is also shown in Figure 11 (top). The difference between the maximum and minimum deviations, when comparing the tweaked and ideal responses, yields a ripple for frequencies below 650 MHz of only 2.75 dB.

Net Result

To observe the overall compensation, we imported the measured two-port parameters of

the compensator into Microwave Office, placed this in cascade with the SLED, and measured the resultant $|\mathbf{S}_{21}|$ response. A graphical comparison of the uncompensated, ideal, simulated, and measured compensation is shown in Figure 11 (bottom). Figure 11 indicates that the 3 dB point of the SLED was increased from 340 MHz to 550 MHz, and the overall response dip was decreased from over 30 dB to less than 12 dB, which constitutes significant improvement. It is also important to note that the phase response of the compensator had an insignificant slope as compared to the phase of the SLED, and thus the compensator preserves phase linearity. Even without the additional tuning, the compensator would have improved the SLED response significantly. Overall, the compensator shows a small-scale, cost-effective means of correcting for the poor modulation response of the SLED, which is of much utility when attempting to broadcast over WDM PON networks.

Figures

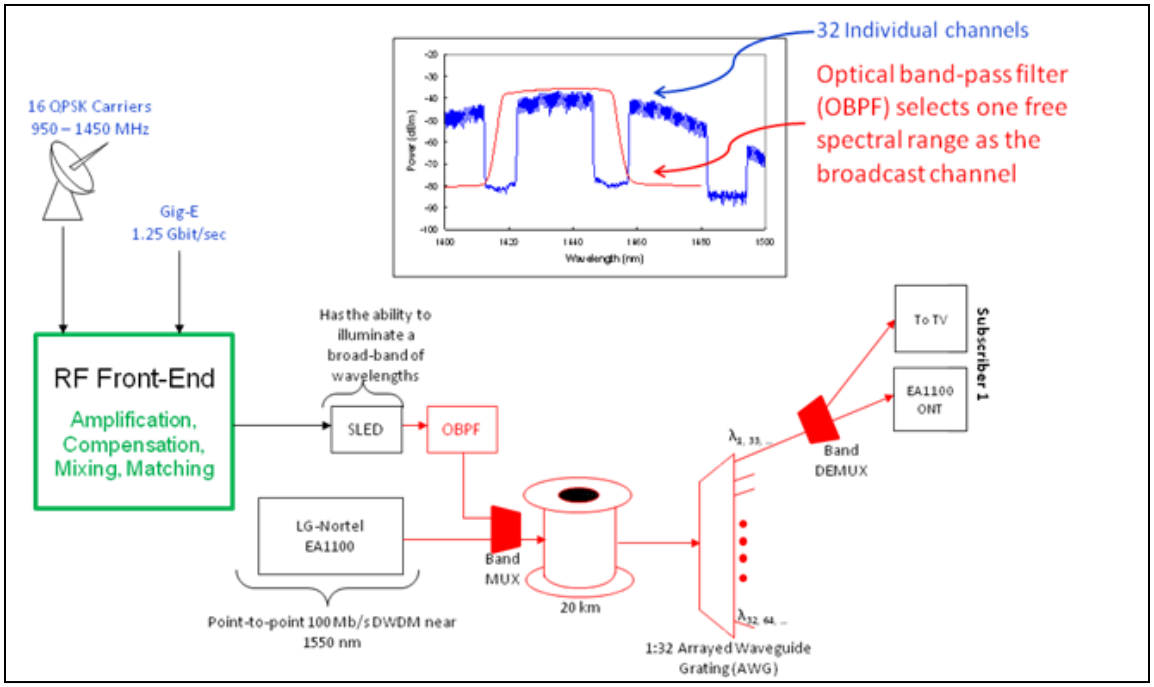

Figure 1: Broadcast service addition to a WDM PON network showing the necessary RF Front-End circuitry before the SLED.

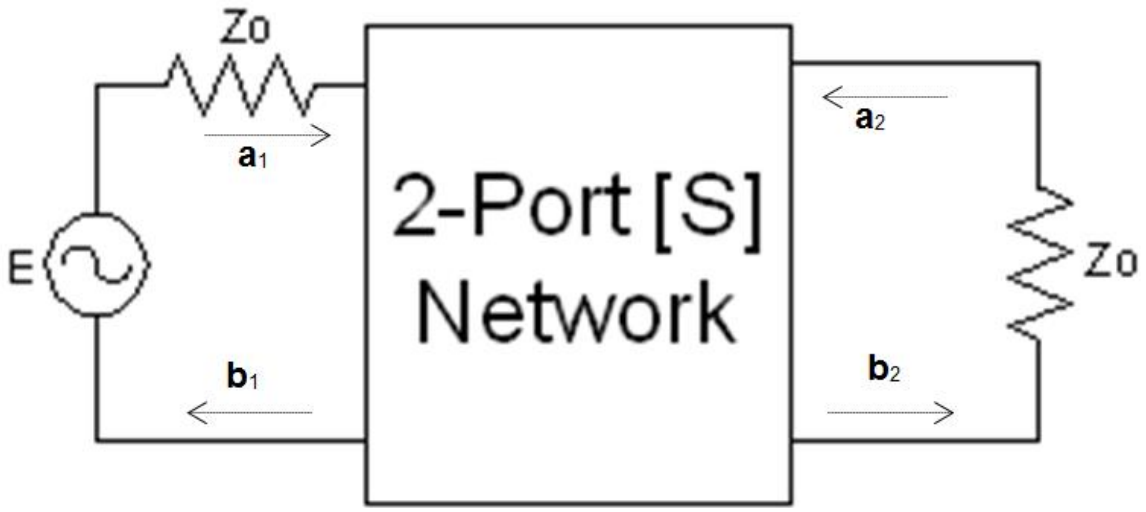

Figure 2: 2 port network represented by its S-matrix in terms of incident and reflected waves.

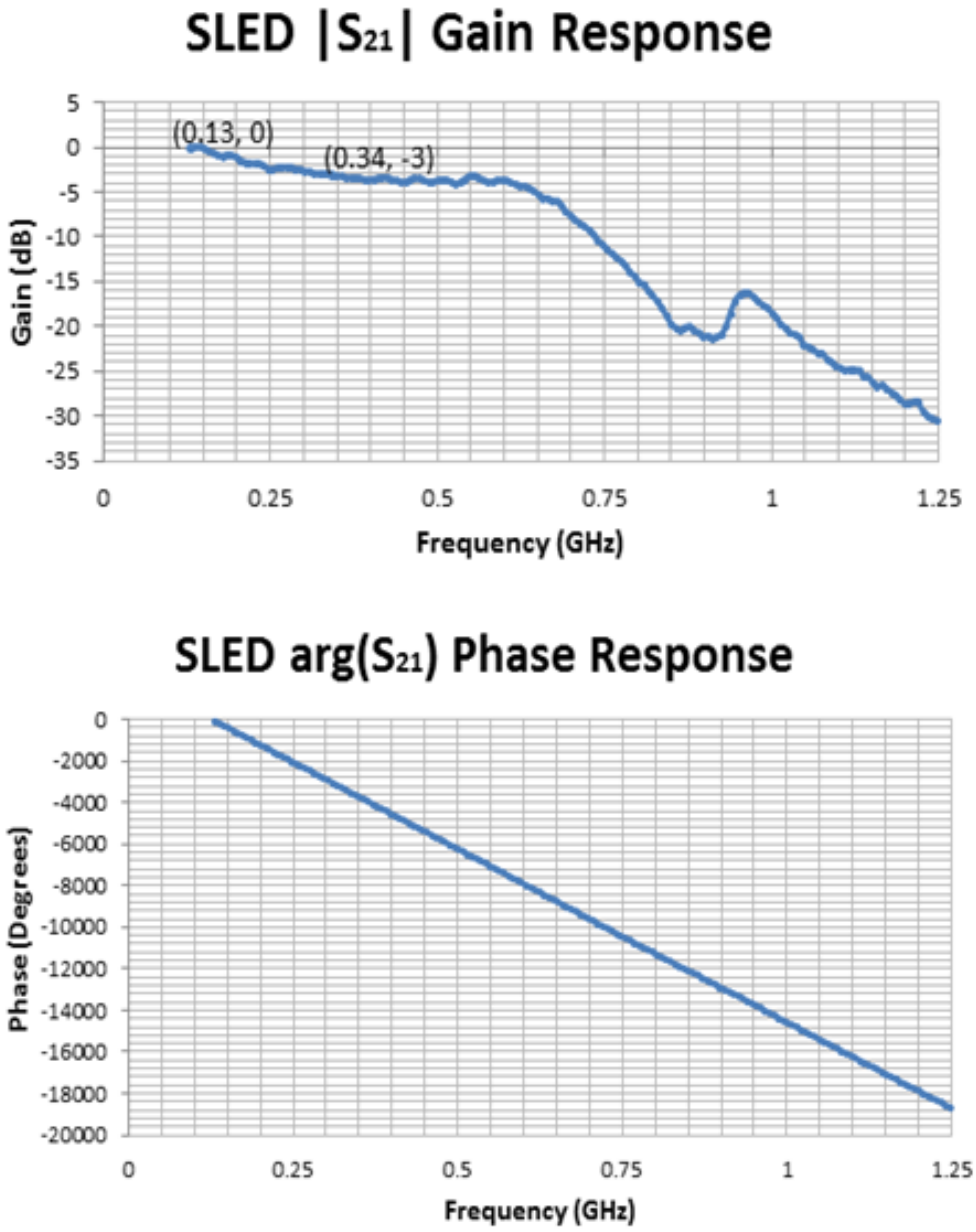

Figure 3: SLED S_{21} magnitude (top) and phase (bottom) response. The gain response shows a 3 dB bandwidth of 340 MHz, and over 30 dB of loss in magnitude over the bandwidth of interest. The phase response is linear.

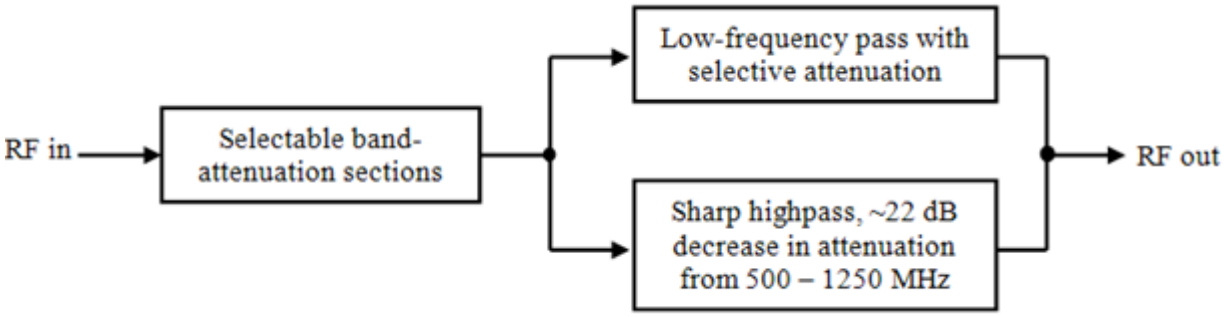

Figure 4: Block diagram showing the overall logic used in developing the compensator stage, disregarding the effect of loading between each of the three stages.

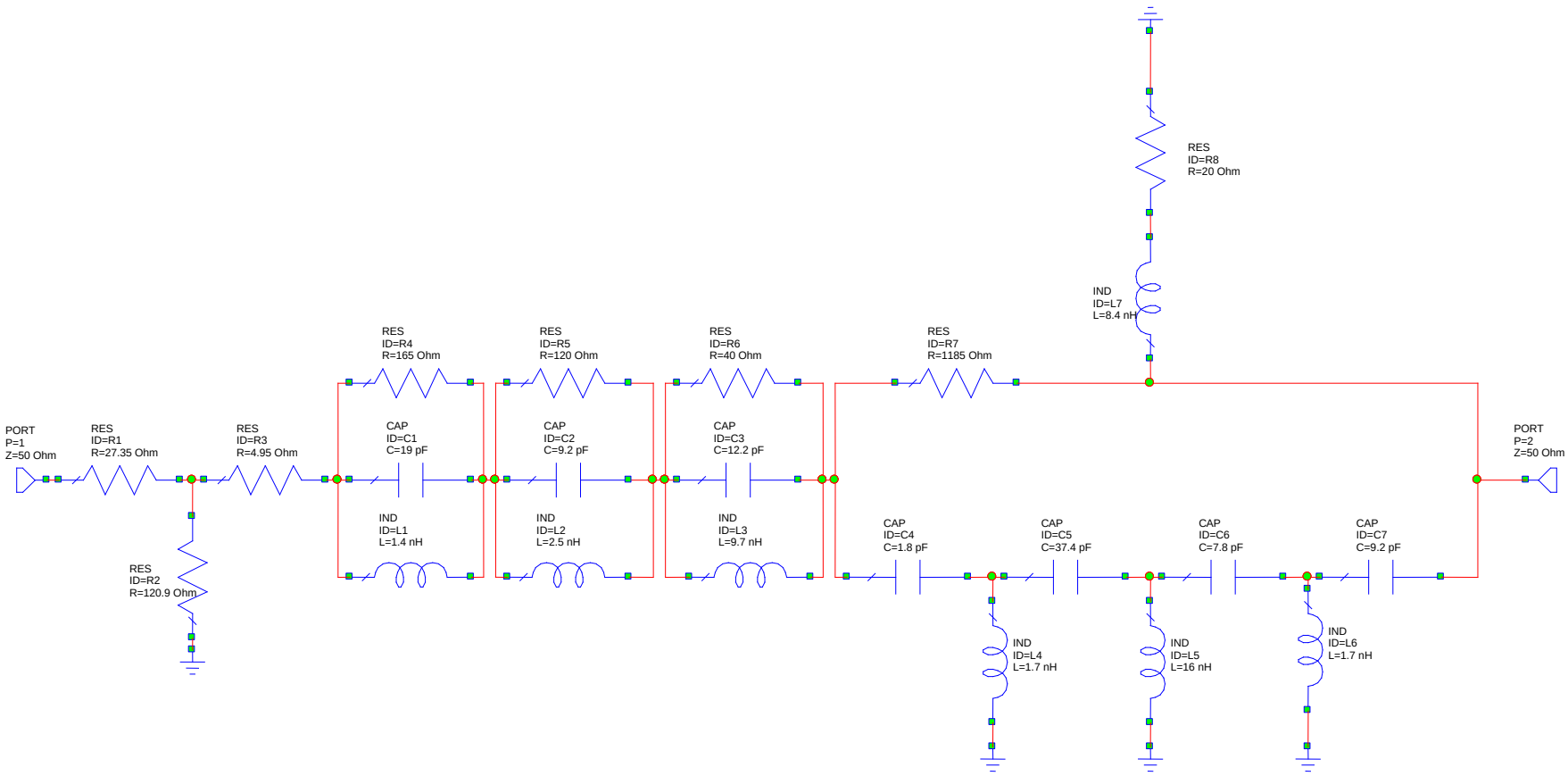

Figure 5: Compensator design using ideal circuit components.

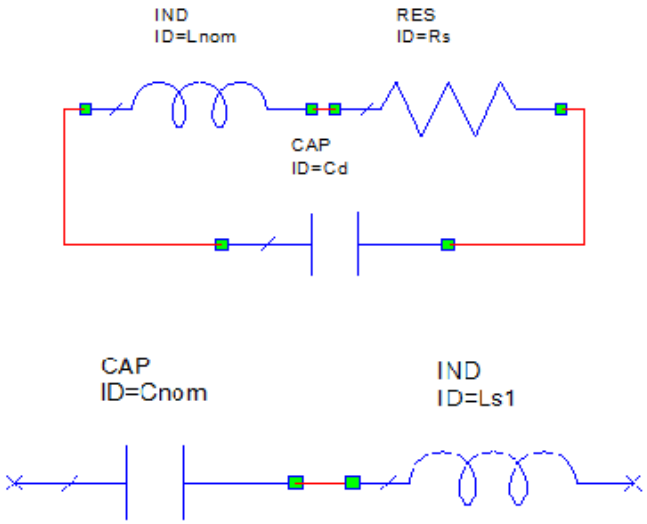

Figure 6: Inductor (top) and capacitor (bottom) models, factoring in f_{res} and ESR.

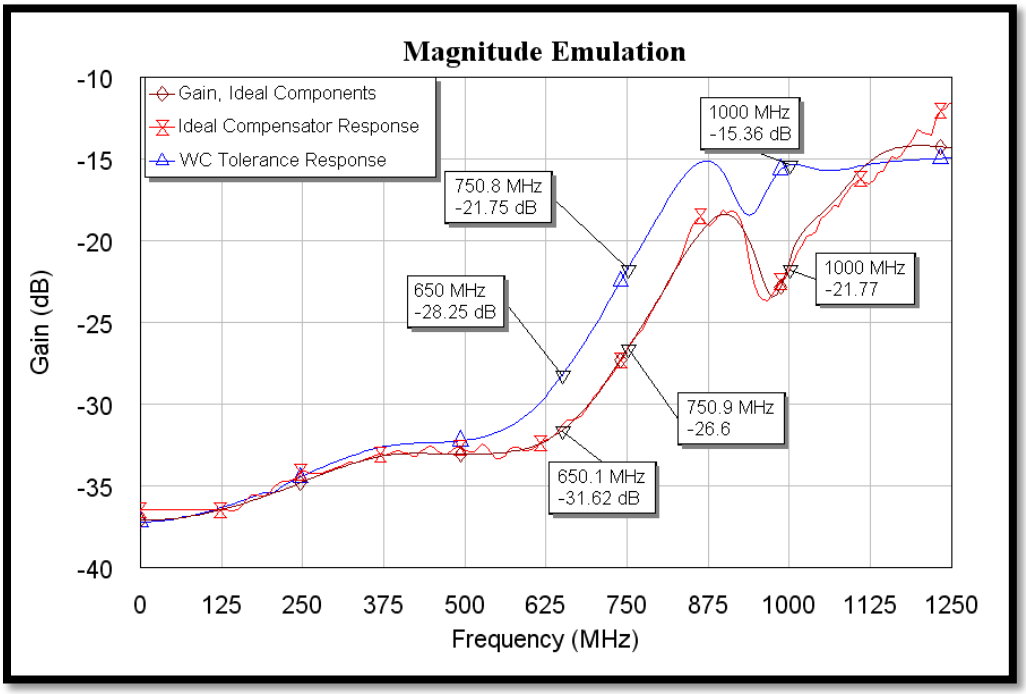

Figure 7: Response factoring in the worst-case tolerances on the inductors. As one can see, at 650 MHz, there is a potential for up to 7 dB of deviation.

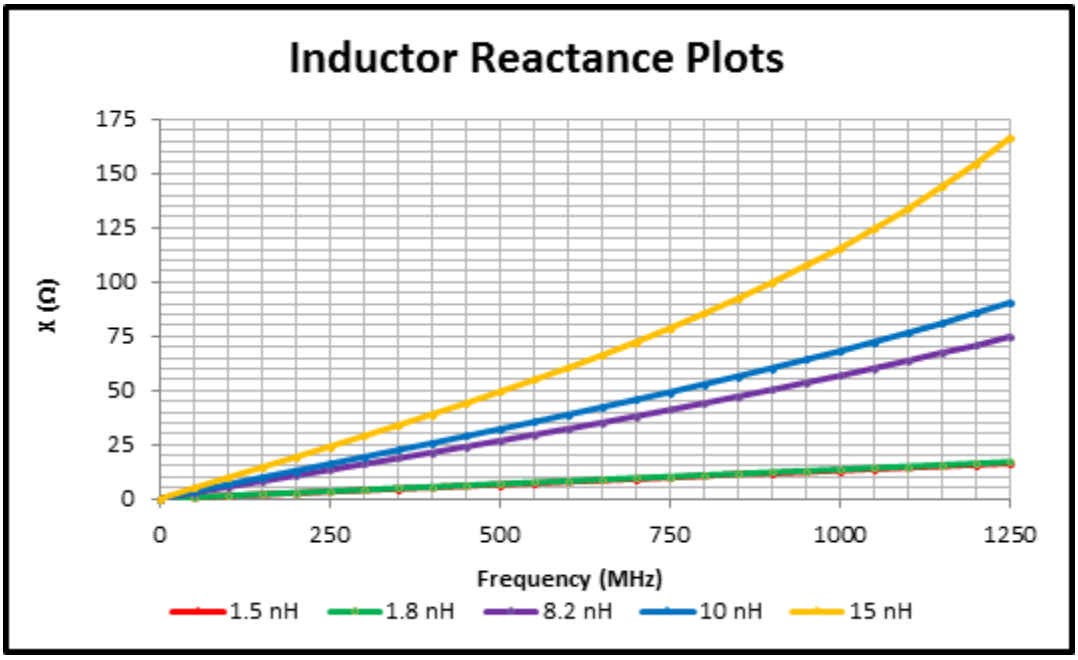

Figure 8: Measured inductor reactance plots. Regressions run on each individual trace all showed a high degree of linearity ($R^2 > 0.997$) with the exception of the 15 nH ($R^2 = 0.98$)

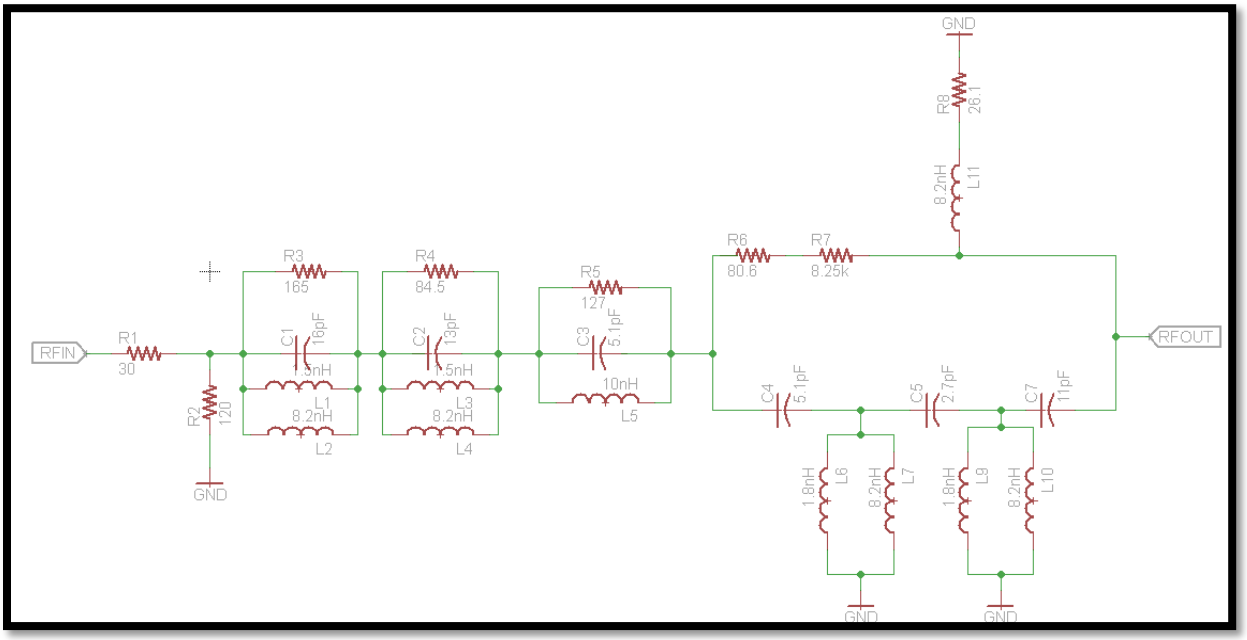

Figure 9: Eagle schematic layout of the compensator.

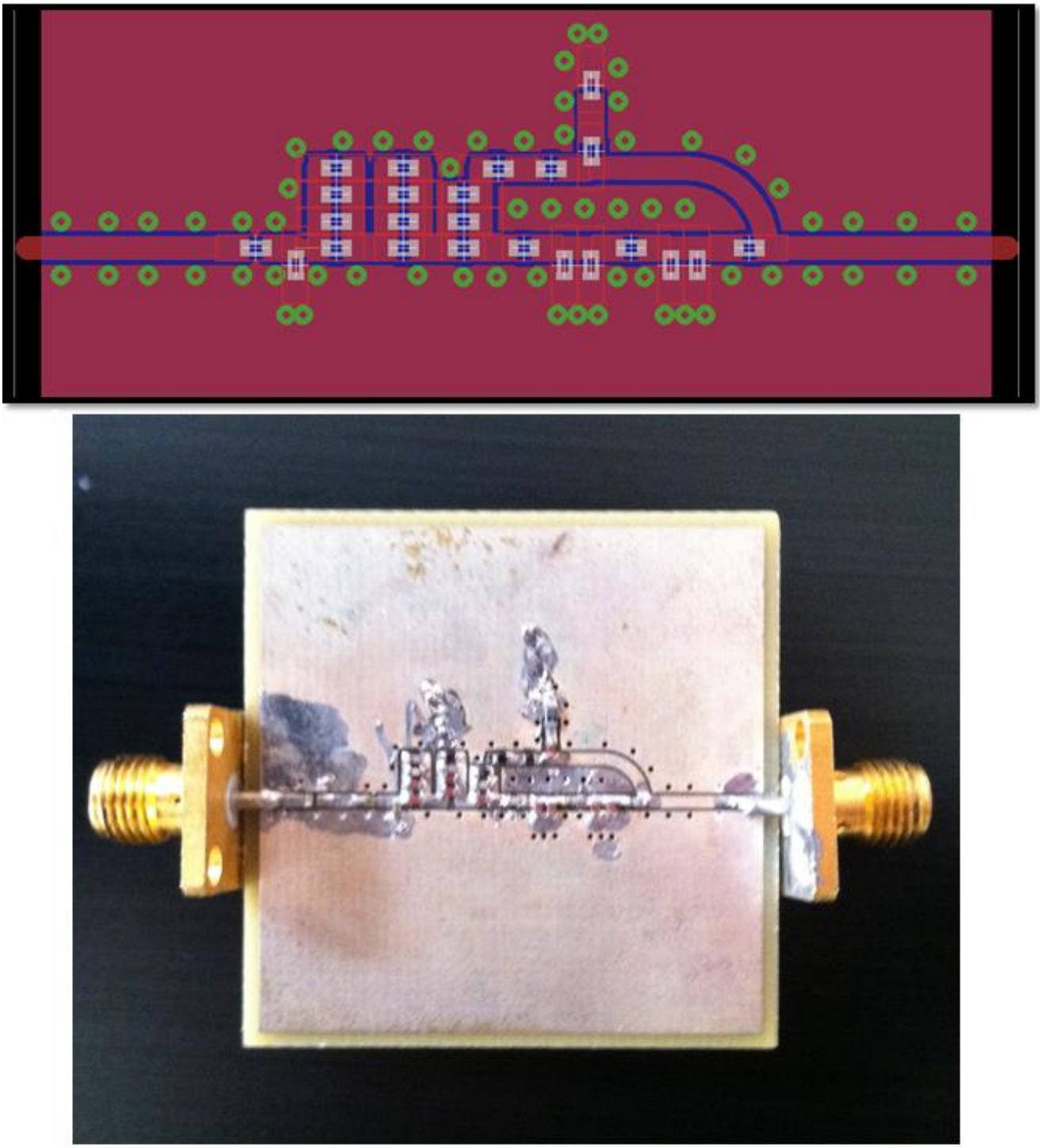

Figure 10: Eagle board layout used to generate Gerber files for etching (top), and fabricated compensator constructed at Linearizer Technology (bottom).

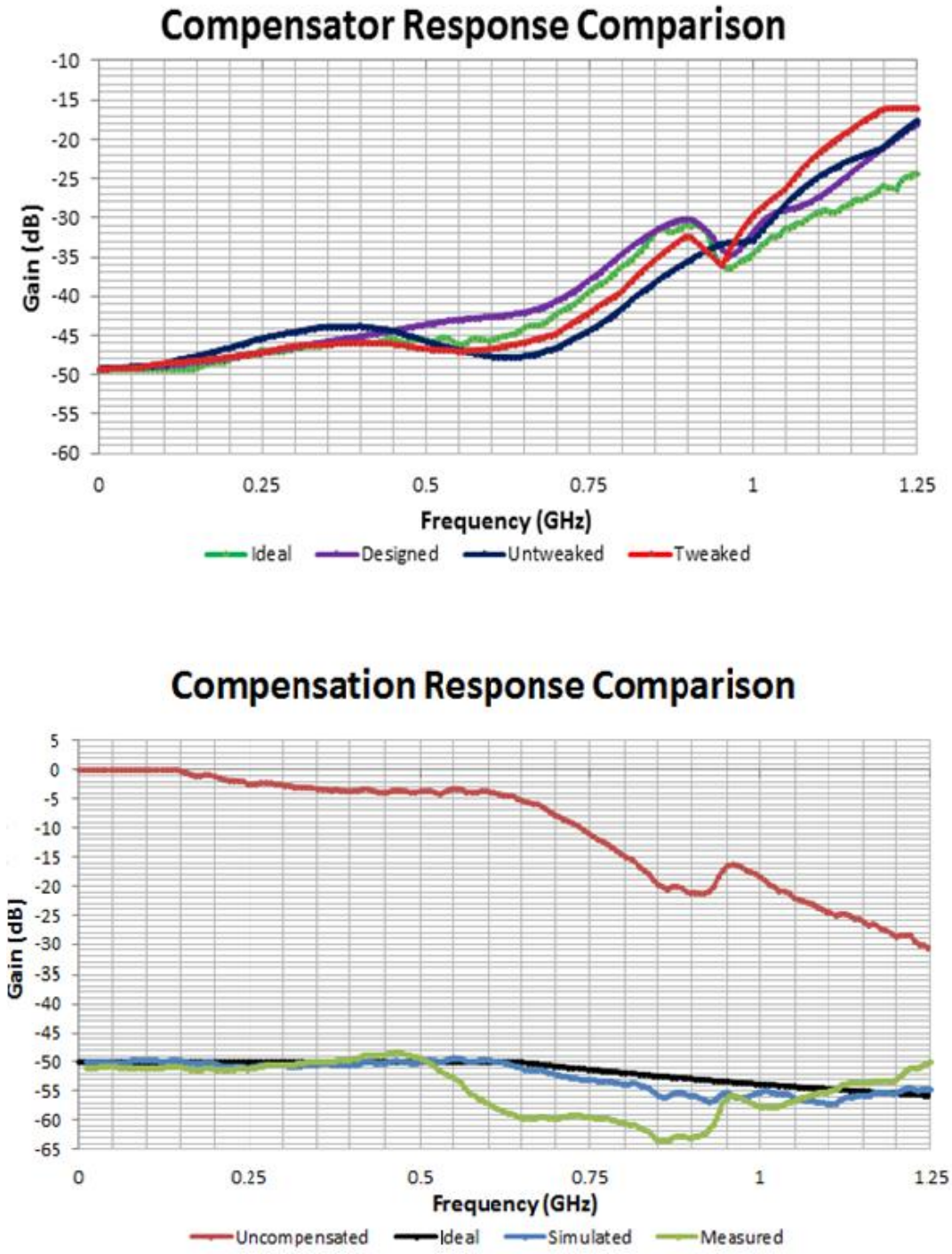

Figure 11: Comparison between the ideal, designed, untweaked, and tweaked compensator responses (top), and between the uncompensated, ideal, simulated, and measured compensation responses (bottom).

Table

Component	**L** (nH) or **C**(pF)	**Tolerance** (± nH or ±pF)	**Q** (X_L/R_s)	**F_r** (MHz)	**FRES** (GHz)	**R_s** @ F_r	**L_s** (nH) or **C_d** (pF)
L1	1.5	0.3	8	100	15	0.1178	0.0751
L2	2.4	0.3			10	0.1885	0.1055
L3	10	0.5			3.7	0.7854	0.1850
L4, L6	1.8	0.3			14	0.1414	0.0718
L5	15	0.75			3.1	1.1781	0.1757
L7	8.2	0.41			4.6	0.6440	0.1460
C1	18	0.18	-	-	4	-	87.95
C3	12	0.12			4		131.9
C4	1.8	0.05			9		173.7
C5	27	0.27			2.5		150.1
C6	7.5	0.1			4		211.1
C2, C7	9.1	0.1			4		174.0

Table 1: Inductors and capacitors selected from Digi-Key Corporation, with L_s and C_d calculations, respectively.

L (nH)	**Measured Inductance** (nH)
1.5	2.10
1.8	2.18
8.2	9.34
10	10.89
15	20.2

Table 2: Measured inductances vs. nominal inductor values.